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# Gradual electroforming and memristive switching in Pt/CuO<sub>x</sub>/Si/Pt systems

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#### Abstract

We report a memristive switching effect in  $Pt/CuO_x/Si/Pt$  devices prepared by the rf sputtering technique at room temperature. Differently from other Cu-based metal filament switching systems, a gradual electroforming process, marked by a gradual increase of the device resistance and a gradual decrease of the device capacitance, was observed in the current–voltage and capacitance characteristics. After the gradual electroforming, the devices show a uniform memristive switching behavior. By Auger electron spectroscopy analysis, a model based on the thickness change of the SiO<sub>x</sub> layer at the CuO<sub>x</sub>/Si interface and Cu ion migration is proposed for the gradual electroforming and uniform memristive switching, respectively. This work should be meaningful for the preparation of forming-free and homogeneous memristive devices.

S Online supplementary data available from stacks.iop.org/Nano/24/325202/mmedia

(Some figures may appear in colour only in the online journal)

## 1. Introduction

Nanoionics-based memristive devices (NIMDs) have attracted intensive attention in recent years due to their potential application in resistive random access memory (RRAM) as well as reconfigurable logic devices [1, 2]. The basic structure of an NIMD consists of an electrode/electrolyte/electrode sandwich structure. According to the charge type of the active ions in switching, NIMDs can be classified into two categories: cation-based devices and anion-based devices. The typical active cations are Cu<sup>2+</sup> and Ag<sup>+</sup>, and the familiar anion is  $O^{2-}$ . The transport of  $O^{2-}$  is equivalent to that of an oxygen vacancy. Many kinds of material can be used as the electrolyte, such as GeSe [3], CuS [4], SiO<sub>2</sub> [5] and  $TaO_x$  [6] with metal ions, and  $TiO_{2-x}$  [7],  $SrTiO_{3-x}$  [8],  $Cr-SrTiO_{3-x}$  [9] and  $Pr_{0.7}Ca_{0.3}MnO_{3-x}$  [10] with oxygen vacancies. For cation-based NIMDs, two processes, ion drift and redox at the anode/cathode, generally occur under an

external electric field, leading to metal filaments in the electrolyte [1-6, 11]. Memristive switching is realized by connection and rupture of the metal filament. Although the detailed processes are still under debate [11, 12], they are believed to be stochastic in nature, resulting in non-uniformity of the switching parameters [2]. Moreover, the scaling potential of the NIMD suffers from the tiny size of the filament, which will lead to a large current density in the switching process as well as for the selector devices [13]. Due to these drawbacks, NIMDs without uncontrollable filaments are desirable for super-integrated devices. In this paper, we present an investigation on a Cu-based NIMD with the structure  $Pt/CuO_x/Si/Pt$ . This device displays a special electroforming accompanied by a gradual increase of the device resistance and a gradual reduction of the device capacitance, and then a uniform memristive switching. Based on analysis of the valence state of each element around the interface after repeated resistance switching, the physical



**Figure 1.** (a) I-V characteristics of the Pt/CuO<sub>x</sub>/Si/Pt devices with a current compliance of 10 mA. Inset: schematic of the device and measurement. (b) Retention behavior of the HRS and LRS under a reading voltage of 0.4 V. (c) Variation of the resistance values in the HRS ( $R_{\text{HRS}}$ ) and LRS ( $R_{\text{LRS}}$ ) as a function of the switching cycles. Inset: variation of  $R_{\text{HRS}}/R_{\text{LRS}}$  and the rectifying ratio in the LRS. (d) Resistance variation as a function of the electrode area. The resistances were read from five electrode points for each electrode area in the same devices with a reading voltage of 0.4 V after the GE process. Dashed curves are the reference for the resistance inversely proportional to the electrode area.

mechanism of the special electroforming and memristive switching is discussed.

#### 2. Experiment

Samples were prepared by the technique of radio-frequency magnetron sputtering at ambient temperature. A Si layer of 40 nm in thickness was first deposited on a commercial Pt/Ti/SiO<sub>2</sub>/Si substrate in an Ar atmosphere of 1 mTorr. Then a CuO<sub>x</sub> layer of 25 nm was deposited in an Ar/O<sub>2</sub> mixed gas atmosphere of 5 mTorr with Ar:O=5:1. As top electrode, a Pt layer of 30 nm was finally deposited in an Ar atmosphere of 5 mTorr. The Pt/CuO<sub>x</sub> layers were patterned, by the photolithography and lift-off technique, as square arrays with sizes ranging from 75  $\times$  75 to 175  $\times$  175  $\mu$ m<sup>2</sup>. The as-deposited Si and  $CuO_x$  layers were determined to be amorphous since no peaks can be observed in the x-ray diffraction spectra (see figures S1 and S2 in the supplementary data available at stacks.iop.org/Nano/24/325202/mmedia). For comparison, devices with stack structures of  $Pt/CuO_x(25 \text{ nm})/Pt$  and Pt/Si(40 nm)/Pt were also prepared under the same conditions. The current-voltage (I-V) characteristics were measured using a Keithley 2601 sourcemeter. Electric polarity directed from the top to the bottom electrode was defined as positive. Impedance spectroscopy in the frequency range

of 40 Hz–110 MHz was measured by an Agilent 4294 A precision impedance analyzer under an ac bias of 0.4 V. The depth profile and the chemical compositions of the CuO<sub>x</sub>/Si interfaces were analyzed by an Auger electron spectrometer at a sputtering rate of 4.4 nm min<sup>-1</sup>. All of the measurements presented in this paper were taken on devices with electrode sizes of  $125 \times 125 \ \mu\text{m}^2$  and all of the device resistances were read under a dc bias of 0.4 V except when otherwise specified.

# 3. Results and discussion

Figure 1(a) shows the *I*–*V* characteristics of the Pt/CuO<sub>x</sub>/Si/Pt device, obtained by cycling dc bias according to  $0 V \rightarrow +4 V \rightarrow 0 V \rightarrow -4 V \rightarrow 0 V$  at a ramping speed of 0.2 V s<sup>-1</sup>. A current compliance (*I*<sub>com</sub>) of 10 mA was selected to avoid permanent breakdown. The *I*–*V* curves exhibit a pronounced electric hysteresis, which is a signature of memristive switching. The device transited from a high resistance state (HRS) to a low resistance state (LRS) with increase of positive bias and switched back after the sweeping of negative bias. The high to low resistance ratio, recorded under a voltage bias of 0.4 V, was larger than 10<sup>2</sup> even after 100 cycles (inset in figure 1(c)). Figure 1(b) shows the typical retention behavior of the device under a reading voltage of 0.4 V. The resistance in the HRS showed small fluctuations



**Figure 2.** (a) I-V curves for the Pt/CuO<sub>x</sub>/Pt, Pt/Si/Pt, and Pt/CuO<sub>x</sub>/Si/Pt devices in the IRS. (b) I-V curves for the Pt/CuO<sub>x</sub>/Si/Pt devices in the HRS and LRS after 100 switching cycles, and the LRS 100 s after 100 switching cycles.

around  $10^7 \Omega$  up to  $3 \times 10^4$  s, whereas the resistance in the LRS exhibited a gradual increase with time from  $6 \times 10^5$  to  $1 \times 10^7 \Omega$ . The final state of the LRS can be considered as a failure state because the resistance value of the LRS was near to the initial value of the HRS. Usually the failure mode of the LRS in filament-based memristive switching shows an abrupt increase due to the rupture of dominant metal filaments. No abrupt resistance increase was observed in the LRS, implying that there were no so-called dominant metal filaments formed in the devices.

In general, a so-called electroforming process is needed for filament-based memristive switching. In this process, the device shows an abrupt switching from the initial resistance state (IRS) to a low resistance state, and this switching needs an electric field higher than that for the following switchings [3–6, 13]. Moreover, the resistance of the HRS is always lower than that of the IRS in the following switching because some of the filaments still exist in the HRS. However, this type of electroforming did not appear in the Pt/CuO<sub>x</sub>/Si/Pt devices. As shown in figure 1(a), the device exhibited a smooth I-V relation, especially for the first few electric cycles, and no obvious abrupt resistance switching was observed. Meanwhile, the I-V loops underwent a gradual downward shift with electric cycling, which is an indication of progressive resistance growth, and stable I-Vloops were obtained only after about 30 electric cycles. This means that the electroforming process lasts for about 30 cycles to stabilize the memristive switching. To distinguish from the process reported previously, we call this type of electroforming process gradual electroforming (GE).

The GE assigns the device three electric behaviors different from those yielded by the electroforming that generates a conductive filament. First, the resistances of both the HRS and LRS increase with I-V cycling (figure 1(c)). As a consequence, the resistance of the HRS is larger than that of the IRS. Second, the I-V characteristics in the LRS are non-linear and evolve from symmetry to asymmetry after repeated electric cycles. As shown in the inset of figure 1(c), the ratio of the resistances read under 0.4 V and -0.4 V, respectively, grew from ~1.2 to ~10 after the first five cycles and then became stable. Third, the resistance values of both the HRS and the LRS after the GE show an inversely

proportional dependence on electrode area (figure 1(d)), which is an indication of uniform switching.

To examine which component of the device is responsible for the memristive switching, the I-V characteristics of the Pt/CuO<sub>x</sub>/Pt and Pt/Si/Pt devices were also studied. As shown in figure 2, both the  $Pt/CuO_x/Pt$  and the Pt/Si/Ptdevices exhibit linear-like I-V relations, indicating the Ohmic character of the  $Pt/CuO_x$  and Si/Pt contacts. The device resistances are  $\sim 51$  and  $\sim 36 \Omega$  for the Pt/CuO<sub>x</sub>/Pt and Pt/Si/Pt devices, respectively, significantly lower than that of the Pt/CuO<sub>x</sub>/Si/Pt devices (~1 MΩ). CuO<sub>x</sub> is a high-conductance semiconductor and the high conductance can be ascribed to oxygen vacancies. Usually, amorphous Si has a high resistivity of  $\sim 10^5 \Omega$  cm, corresponding to about 1 k $\Omega$  for our devices. The lower resistance may originate from structural defects. The Si layer is actually composed of relatively incompact nanometer-sized ( $\sim$ 70 nm) grains (see figure S3 in the supplementary data available at stacks. iop.org/Nano/24/325202/mmedia). By comparing the three devices, we came to the conclusion that the high resistance of  $Pt/CuO_x/Si/Pt$  arose from the  $CuO_x/Si$  interface, and it is this interface that is responsible for the memristive effect.

Besides resistance switching, a capacitance switching was also observed in the  $Pt/CuO_x/Si/Pt$  device. Figure 3 shows the typical impedance spectra of the IRS, HRS, and LRS. The impedance spectra can be well fitted by an equivalent circuit consisting of one parallel R and C in series with a resistor ( $R_0$ ).  $R_0$  is lower than 40  $\Omega$ , representing the resistance from electrode contacts, leading wires, and the body of the device, while the parallel R and C mimic the  $CuO_x/Si$  interface. The capacitances obtained from the impedance spectra are 210 pF. 140 pF, and 170 pF for the IRS, HRS, and LRS, respectively. The capacitance of the LRS was always larger than that of the HRS, which could be an indication of a reduction of the effective thickness of insulating layer at the CuO/Si interface. Corresponding to the GE, as illustrated in figure 4(a), the capacitance in either the HRS ( $C_{\text{HRS}}$ ) or the LRS ( $C_{\text{LRS}}$ ) showed a gradual decrease with 30 electric cycles.

There are possible reasons for the high resistance of the  $CuO_x/Si$  interface as well as the electric cycle-induced resistance/capacitance change. The first one is the presence of an interfacial barrier. As is well established, an interfacial barrier favors rectifying I-V characteristics. However, the



**Figure 3.** Cole–Cole plots of the Pt/CuO/Si/Pt device in the IRS, HRS, and LRS. Inset: the equivalent circuit for curve fitting. The data used for fitting are  $R_0 = 18 \Omega$ ,  $R_{\text{HRS}} = 1.11 \text{ M}\Omega$ ,  $C_{\text{HRS}} =$ 140 pF,  $R_{\text{LRS}} = 87.8 \text{ k}\Omega$ ,  $C_{\text{LRS}} = 170 \text{ pF}$ ,  $R_{\text{IRS}} = 670 \text{ k}\Omega$ , and  $C_{\text{IRS}} = 210 \text{ pF}$ .

*I–V* curves in the HRS and IRS are symmetric (figure 2) when the measurement is performed within a bias range between -1 V and +1 V to avoid resistance switching. Although the *I–V* curve in the LRS is asymmetric, it becomes symmetric 100 s after switching to the LRS (figure 2(b)). This implies that the rectification shown in figure 1(a) is a metastable behavior rather than an effect due to the interfacial barrier. In other words, the existence of the interface barriers can be excluded. Another reason is the formation of an insulating interfacial layer. According to the formation energies of CuO (-129.7 kJ mol<sup>-1</sup>), Cu<sub>2</sub>O (-146 kJ mol<sup>-1</sup>), SiO (-342 kJ mol<sup>-1</sup>), Si<sub>2</sub>O (-426 kJ mol<sup>-1</sup>), and SiO<sub>2</sub> (-911 kJ mol<sup>-1</sup>) [14, 15], the following chemical reactions could take place spontaneously around the CuO<sub>x</sub>/Si interface:

$$2\operatorname{CuO}_{x} + \operatorname{Si} \to \operatorname{Cu}_{2}\operatorname{O} + \operatorname{SiO}_{x};$$
  

$$\operatorname{CuO}_{x} + \operatorname{Si} \to \operatorname{Cu} + \operatorname{SiO}_{x}.$$
(1)

It is therefore possible to form a transitional layer containing  $SiO_x$ , Cu, and Cu<sub>2</sub>O at the CuO<sub>x</sub>/Si interface in the process of sample preparation and the following electric cycling.

In order to verify this conclusion, the composition and chemical states of the CuOx/Si interface were investigated by AES depth analysis. Figures 5(a) and (b) show the AES depth profile spectra of the  $CuO_x/Si$  interfaces in the IRS and HRS(100), where HRS(100) is the HRS after  $10^2$  cycles of  $0 \rightarrow 4 \rightarrow -4 \rightarrow 0$  V. As expected, a transitional layer consisting of Cu, Si, and O was detected at the CuO<sub>x</sub>/Si interface. The valence states of Cu and O at various depths can be determined based an analysis of the line shape in the AES spectra. As shown in figures 5(c)-(f), the kinetic energy of the Cu LMM decreased from 915 eV (Cu<sup>2+</sup>) to 914 eV (Cu<sup>+</sup>) and then to 916 eV (Cu<sup>0</sup>) when the depth extended from the CuO<sub>x</sub> layer to the  $CuO_x/Si$  interface in both the IRS and HRS(100), indicating a progressive reduction of  $Cu^{2+}$  to  $Cu^{+}$  and then  $Cu^0$  [16]. Correspondingly, the kinetic energy of the O KLL decreased from 511 eV (CuO) to 506 eV (SiO<sub>x</sub>) [17]. These results are consistent with the chemical reactions described by equation (1), and demonstrate the emergence of a  $SiO_x$  layer around the  $CuO_x/Si$  interface, coexisting with  $Cu_2O$  and Cu.

The AES spectra also revealed a thickness change of the SiO<sub>x</sub> layer from  $\sim$ 5 to  $\sim$ 7 nm when the resistive state of the device switched from IRS to HRS(100). We also measured the AES spectra of the LRS(100). However, no difference between the HRS(100) and LRS(100) can be distinguished, which indicates stabilization of the interfacial layer after 100 electric cycles. These results are consistent with the capacitance decrease with electric cycling. The capacitance is closely related to the  $SiO_x$  layer thickness according to the formula  $d = \varepsilon_0 \varepsilon_r S/C$ , where d is the layer thickness,  $\varepsilon_r$  is the relative permittivity,  $\varepsilon_0$  is the vacuum permittivity, and S is the electrode area. However, the exact value of  $\varepsilon_r$  was unknown here, because it is related with the exact composition and structure of the  $SiO_x$  layer and might vary with the resistance switching. Therefore, we calculated the effective thickness  $d' = d/\varepsilon_{\rm r}$ . To some extent, if  $\varepsilon_{\rm r}$  changes little, d' can also reflect the real thickness change of the  $SiO_x$  layer either in the HRS or in the LRS with switching cycles. As shown in



**Figure 4.** Variation of (a) the capacitance of the Pt/CuO<sub>x</sub>/Si/Pt devices and (b) the calculated effective thickness d' as a function of switching cycles.  $d' = d/\varepsilon_r = \varepsilon_0 S/C$ , where d is the layer thickness,  $\varepsilon_r$  is the relative permittivity,  $\varepsilon_0$  is the vacuum permittivity, and S is the electrode area.



**Figure 5.** (a), (b) The AES depth profile spectra at the  $CuO_x/Si$  interface in the IRS and HRS(100), respectively. (c), (d) The AES line shape analysis of the Cu *LMM* in the IRS and HRS(100), respectively. (e), (f) The O *KLL* in the IRS and HRS(100), respectively. Lines from a to g identify the different depths.

figure 4(b), the effective thickness d' first grew from ~0.68 to ~0.89 nm in the LRS and from ~0.79 to ~0.90 nm in the HRS during the first ~30 cycles corresponding to the GE. With further cycling, it became relatively stable and its difference in the LRS and HRS diminished progressively, and was almost negligible above ~50 cycles.

The mechanism for memristive switching in Cu/ electrolyte systems with electrolytes of SiO<sub>2</sub> [5], Ta<sub>2</sub>O<sub>5</sub> [6], GeO<sub>x</sub> [18], ZnO [19], and HfO<sub>2</sub> [20], has been reported, and the formation and rupture of the Cu filament that links the top and bottom electrodes was believed to be responsible for the resistance change. However, this model cannot explain the GE, the capacitance switching, and the uniform memristive switching effects occurring in the Pt/CuO<sub>x</sub>/Si/Pt devices. According to the experimental results, a model based on drift of Cu<sup>z+</sup> and oxidation of Si at the CuO<sub>x</sub>/Si interface is proposed as follows.

In the IRS, a  $SiO_x$  layer was formed at the  $CuO_x/Si$ interface in the process of sample preparation, resulting in a high initial resistance value (figure 6(a)). Driven by the positive biases, the  $Cu^{z+}$  ions migrated from the  $CuO_x$  layer through the  $SiO_x$  layer, and then accumulated at the Si layer surface due to the lower mobility of  $Cu^{z+}$  in Si than in  $SiO_x$  [21]. At the same time, oxygen vacancies could also be driven into the  $SiO_x$  layer. Due to the large lattice defects as well as the large specific surface of the incompact amorphous Si layer, the solubility of Cu in the Si layer could be relatively high. The amorphous Si layer acted as an ion sink and suppressed the Cu atom precipitation [22]. Therefore, differently from the so-called Cu-metal filament systems, Cu existed in the SiO<sub>x</sub> layer as ions rather than metal atoms. The Cu<sup>z+</sup> acted as trapping centers of electrons, providing additional paths for electrons tunneling through the  $SiO_x$  layer. Due to the relatively high resistance induced



**Figure 6.** Schematics of the proposed chemical (top) and electronic (bottom) modifications between (a) the IRS, (b) the first LRS, (c) the first HRS, and (d) the second LRS of the memristive switching in the  $Pt/CuO_x/Si/Pt$  devices. For simplicity, the oxygen vacancies are expressed by the oxygen ions (O<sup>2-</sup>).

by the tunneling process, the accumulation of electric field around the  $Cu^{z+}$ , which moved faster than others, was weak, and hence  $Cu^{z+}$  migrated relatively uniformly into the  $SiO_x$  layer. However, completely uniform migration might not be possible. Under the electric field the electrons will inevitably prefer to tunnel through some sites with higher  $Cu^{z+}$  concentration in the SiO<sub>x</sub> layer, forming multi-tunneling filaments. Note that the Cu<sup>+</sup> and Cu<sup>0</sup> already existed in the  $SiO_x$  layer even before the electroforming operation according to the AES data. As a result, plenty of tunneling filaments could be formed simultaneously in the  $SiO_x$  layer, yielding a uniform resistance switching. It should be pointed out that the uniform switching was only demonstrated within certain range of electrode sizes. With scaling down of the device size to a size comparable to the tunneling filaments, some filamentary switching behavior might appear. Further studies, such as the memristive switching characteristics in nanoscale devices, are still required to elucidate the switching homogeneity.

Under negative bias, the  $Cu^{z+}$  moved back to the  $CuO_x$ layer and, in the meantime, the oxygen vacancies migrated out of the  $SiO_x$  layer. The latter, which was equivalent to introducing  $O^{2-}$  into SiO<sub>x</sub>, caused a further oxidation of SiO<sub>x</sub> and thus a growth in the  $SiO_r$  layer thickness (figure 6(c)). Consequently, the HRS showed a higher resistance than the IRS. When applying the next positive bias,  $Cu^{z+}$  and oxygen vacancies migrated into the  $SiO_x$  layer again. However, it was difficult to totally extract the previously incorporated  $O^{2-}$  from the SiO<sub>x</sub> layer due to the strong Si–O bonding as well as the low formation energy of  $SiO_x$ . This means that the  $SiO_x$  layer became thicker than that of the last LRS (figure 6(d)), and, therefore, the resistance value in the LRS increased. When the device was driven to the next HRS, the  $SiO_x$  layer became even thicker and the resistance value of the HRS increased again. Consequently, a gradually growth in the  $SiO_x$  layer thickness, and thus in the resistance, took place

with electric-field cycling. This process corresponds to the GE (figure 1(c)). After the GE, a relatively stable  $SiO_x$  layer was formed, and further electric-field cycling only caused minor changes in the  $SiO_x$  layer thickness. The thickness change of the  $SiO_x$  layer in this model fits well with that of the calculated effective thickness (figure 4(b)), and thus explains the capacitance switching.

The relaxation of the LRS with time (figure 1(b)) can be attributed to a self-diffusion of  $Cu^{z+}$  out of  $SiO_x$ due to its high concentration in  $SiO_x$ . With decrease of the Cu ion concentration in the  $SiO_x$  layer, the electron tunneling became difficult. That can be seen as the rupture of the tunneling filaments. Due to the coexistence of many tunneling filaments in one switching cell of the devices, the abrupt resistance change was masked by the parallel effect among the tunneling filaments, resulting in a gradual increase of the resistance in the LRS with time. The ion diffusion induced by the concentration gradient can also be used to explain the metastable rectifying behavior observed in the LRS (figure 1(a)). Since the  $Cu^{z+}$  diffusion would be enhanced under negative bias, it accelerated the device resistance increase, inducing a rectifying behavior in the LRS. After waiting for 100 s after switching to the LRS, the Cu<sup>z+</sup> self-diffusion was almost completed, and the *I*-*V* curve became stable and non-rectifying (figure 2). From the point of view of memory devices, the instable LRS as well as GE is undesired. Improvement of these properties could be expected by, for example, preparing an inert layer at the  $CuO_x$ /Si interface where further oxidation can be avoided and designing a proper ion diffusion barrier to restrain the ion self-diffusion.

#### 4. Conclusions

In conclusion, we have investigated the memristive switching characteristics of  $Pt/CuO_x/Si/Pt$  devices based on the I-V

curves and capacitance analysis. The devices showed a GE process and a uniform memristive switching behavior. The device resistances in both the HRS and LRS increased with I-V cycling, and the device capacitances decreased gradually before reaching stabilization after the GE process. AES depth analysis revealed the emergence of a SiO<sub>x</sub> layer around the CuO<sub>x</sub>/Si interface, coexisting with Cu<sub>2</sub>O and Cu, and the thickness growth of this layer under external field. Based on the experimental results, we propose that the Cu<sup>2+</sup> and oxygen migration into/out of the SiO<sub>x</sub> layer driven by the electric field is responsible for the memristive switching, and the GE process is attributed to the thickness increase of the SiO<sub>x</sub> layer due to further oxidation under the negative bias condition.

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