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# All-Solid-State Synaptic Transistor with Ultralow Conductance for Neuromorphic Computing

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**Electronic synaptic devices are important building blocks for neuromorphic computational systems that can go beyond the constraints of von Neumann architecture. Although two-terminal memristive devices are demonstrated to be possible candidates, they suffer from several shortcomings related to the filament formation mechanism including nonlinear switching, write noise, and high device conductance, all of which limit the accuracy and energy efficiency. Electrochemical three-terminal transistors, in which the channel conductance can be tuned without filament formation provide an alternative platform for synaptic electronics. Here, an all-solid-state electrochemical transistor made with Li ion–based solid dielectric and 2D $\alpha$-phase molybdenum oxide ($\alpha$-$MoO_3$) nanosheets as the channel is demonstrated. These devices achieve nonvolatile conductance modulation in an ultralow conductance regime (<75 nS) by reversible intercalation of Li ions into the $\alpha$-$MoO_3$ lattice. Based on this operating mechanism, the essential functionalities of synapses, such as short- and long-term synaptic plasticity and bidirectional near-linear analog weight update are demonstrated. Simulations using the handwritten digit data sets demonstrate high recognition accuracy (94.1%) of the synaptic transistor arrays. These results provide an insight into the application of 2D oxides for large-scale, energy-efficient neuromorphic computing networks.**

## 1. Introduction

The rapid rise in electronic data collection and utilization worldwide presents an urgent requirement for computing technology capable of fast and energy efficient processing of information. Conventional processors in which memory and logic functions are separated physically, face an energy-inefficiency challenge stemming from the so-called von Neumann bottleneck, that is, the excessive power required to transfer data between memory and logic.[1] To overcome this, artificial neuromorphic networks based on devices that emulate the functionality of biological neurons and synapses, are being actively investigated for the realization of computational systems that overcome the limitation of von Neumann-based computing systems.[2–9]

In biological brains, the synapse is a functional junction connecting a pair of neurons.[10] Information storage and processing functions are performed in the same synapses by tuning the synaptic weight. Large-scale integrated circuits based on complementary metal–oxide–semiconductor (CMOS) elements have been successfully used to emulate synaptic functions, but face tremendous energy and space cost with increasing complexity. Alternatively, two-terminal memristors have been widely used to emulate synaptic functions.[11–19] However, memristors suffer from several deficiencies such as asymmetric and nonlinear switching in conductance values as well as excessive write noise related to the conductive filament formation mechanism.[20–28] Moreover, memristive devices based on conducting filaments or phase change materials require high write/read currents due to their high conductance, leading to higher request for current capacity, unacceptable voltage drops, and excessive power dissipation on wires as array dimensions increase beyond ≈1000 × 1000. Reducing filament conductance below a quantum conductance $2e^2/h$ (≈77.5 µS corresponding to a single atomic contact, where $e$ and $h$ are the elementary charge and Planck's constant, respectively) without compromising longtime retention and excessive noise has proven difficult.[18,29] These nonidealities constrain the performance, array size, and energy efficiency of the neuromorphic computing networks based on filamentary memristors.

Three-terminal electrochemical transistors (ECT) provides a flexible operation for tuning the device resistance, where the "write" operation is on the gate and the "read" operation is on the source–drain.[30–41] In these devices, the gate dielectric is replaced by electrolytes with mobile ions (e.g., $H^+$, $Li^+$, or $O^{2-}$). By the application of a gate voltage, active ions are injected into the permeable semiconductor channel and change its doping level, modulating thus the conductance of the channel. This operating mechanism without filament formation

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possesses virtues of reversibility, nonvolatility, near-linear analog switching, and low energy consumption, and thus it is favorable for synaptic transistor application. In contrast to the two-terminal memristive devices in which the energy consumption is mainly contributed by the "write" operation, the "read" energy of ECT is comparable or larger than the "write" energy because the gate leakage current is generally much lower than the channel current, and thus the energy efficiency is "read" limited.[31–41] Therefore, it is critical for synaptic transistors with low "read" conductance to reduce overall energy cost of neuromorphic networks composed of large arrays of devices. To enhance the practicality of employing ECTs as synaptic devices, it is highly desirable to use channel materials with inherently low conductivity to construct the devices.

$\alpha$-phase molybdenum oxide ($\alpha$-$MoO_3$) is a layered 2D material which allows the reversible intercalation of cations (e.g., $H^+$ and $Li^+$), via a Faradaic reaction involving the reduction/oxidation of Mo ions.[42–45] It is this mechanism which tunes the oxide electrical properties with minimal structural changes that is in contrast to the filament formation or the melting/recrystallization mechanisms characteristic of the other types of memristors. Compared with graphene and 2D dichalcogenides, $\alpha$-$MoO_3$ has a wide bandgap (≈3 eV) and thus low intrinsic conductivity. $\alpha$-$MoO_3$-based synaptic transistors have been realized in our previous work by using ionic liquid as electrolyte in an appropriate humidity ambience.[37] However, two main drawbacks of such synaptic devices have to be overcome for realizing space-efficient electronic devices. One is the requirement of humidity ambience, in which protons will be generated in the electrolyte and be injected into the channel to play a role of doping. The other one is the use of liquid electrolyte, which limits the high-density integration of devices. From a technological point of view, it is difficult to incorporate liquid phase and environmental factor in the device fabrication and encapsulation, limiting the high-density integration of the devices. To enhance the practicality of employing $\alpha$-$MoO_3$-based ECTs as synaptic devices, it is highly desirable to use solid electrolytes to construct the devices and to perform the synaptic function independent of environment. In this work, we demonstrate an all-solid-state, environment-independent ECT where Li-ion electrolyte is used as the gate dielectric and layered 2D $\alpha$-$MoO_3$ nanosheets are used as the channel. The operation mechanism of the ECT is based on the gate voltage–induced reversible intercalation of Li-ion dopants into $\alpha$-$MoO_3$ lattice, which engenders near-linear modulation of the channel conductance and "read" conductance values sufficiently low to attain high efficiency for large-scale crossbar arrays. The synaptic functionalities of the ECT and the ECT array simulation for image recognition are demonstrated. The implementation of $\alpha$-$MoO_3$-based ECT devices with these functions paves the way for large-scale, energy-efficient neuromorphic computing networks.

## 2. Results and Discussion

### 2.1. Structure and Electrical Properties of $\alpha$-$MoO_3$-Based ECT

The $\alpha$-$MoO_3$ nanosheets with a thickness of 18 nm were prepared by mechanical-exfoliation method, and the gold electrodes were then fabricated on top using standard electron-beam lithography (see **Figure 1**a). Solid electrolyte ($LiClO_4$ dissolved in polyethylene oxide (PEO) matrix) was used as the gate electrolyte, covering both the thin nanosheets and the metal side gate. In this electrolyte, Li ions are easy to move by the relaxation of PEO chains at temperatures far above the glass transition temperature (≈–60 °C).[46] The detailed process of device fabrication is described in the Experimental Section. The electrical measurement setup is schematically illustrated in the inset of Figure 1b. The gate voltage ($V_G$) was directly applied on the gate electrode. Meanwhile, the corresponding channel current ($I_D$) was monitored by applying a small dc voltage ($V_D$ = 50 mV) between the source and drain electrodes. To avoid the ambient humidity impact, all the electrical measurements were performed in a vacuum condition (<$10^{-5}$ Torr).

Figure 1b shows the $I_D$–$V_G$ curves of the devices with $V_G$ sweeping at a rate of 20 mV $s^{-1}$. The devices display a clear counterclockwise hysteresis with a high/low conductance change ratio of ≈1700% at $V_G$ = 0. The large hysteresis indicates a nonvolatile change of the channel conductance, which is essential for the emulation of synaptic functionality. The hysteretic behavior observed here can be understood based on the potential-induced Li-ion intercalation into the $\alpha$-$MoO_3$ nanosheets. Figure 1c–e shows a schematic illustration of this process. When a positive gate voltage was applied (step 1), Li ions in the solid electrolyte were driven toward the channel. The mobile Li ions were first accumulated on the topmost layer of the $\alpha$-$MoO_3$ nanosheet and then were intercalated into the $\alpha$-$MoO_3$ lattice with increasing the gate voltage. The intercalated Li ions acted as dopants in the $\alpha$-$MoO_3$ bulk,[47] contributing free electron carriers and thus the increase of the channel conductance. This process is defined as electrochemical doping and can be described by the following reaction

$$x\mathrm{Li}^+ + x\mathrm{e}^- + \mathrm{Mo}^{6+} \rightarrow x\mathrm{LiMo}_x^{5+}\mathrm{Mo}_{1-x}^{6+}\mathrm{O}_3 \quad (1)$$

where $x$ is the number of injected ions. The valence of Mo ions changes from 6+ to 5+ with the formation of molybdenum bronze ($Li_xMoO_3$).[48] When the gate voltage is reduced from its upper limit 1.5 V (step 2), the internal field ($E_{int}$) built by the concentration gradient of Li ions in the electrolyte becomes gradually dominant and drives the Li ions accumulated on the channel surface back into the electrolyte. Since the molybdenum bronze phase is so thermodynamically stable, a large negative gate voltage is required to extract the Li ions intercalated in the channel, resulting in a hysteresis in the $I_D$–$V_G$ curves. With the negative gate voltage reaching –1.5 V (step 3), Li ions were fully extracted out of the channel and then the $G$ was restored to the initial value.

To clarify the dynamic process of the electrolyte gating, capacitance–frequency ($C$–$f$) measurements of the Au/electrolyte/$MoO_3$ were performed. As shown in **Figure 2**a, the specific capacitance profile can be clearly divided into three regions, a smaller value of ≈7 μF $cm^{-2}$ at high frequency region (>10 kHz), the dramatical increase at frequency region from 0.3 to 10 kHz, and the second increase at frequency region from 0.1 to 0.3 kHz, which correspond to three different types of capacitive behavior. The one in high frequency region (>10 kHz) refers to a bulk electrolyte capacitance, which has a fast charging speed. The capacitance

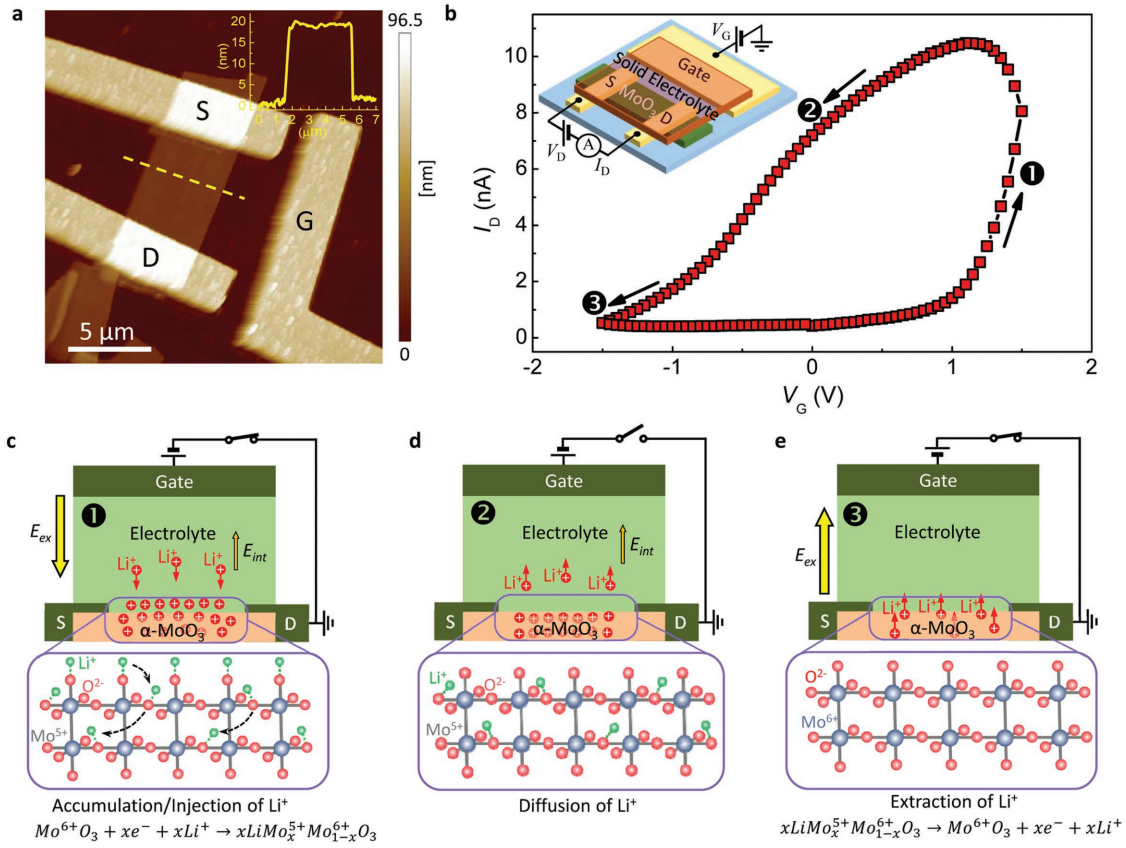


**Figure 1.** a) Atomic force microscopy image of the transistor. The channel between source (S) and drain (D) is made of $\alpha$-$MoO_3$ nanosheet and Li-ion electrolyte is used as the gate. Inset: The line profile of the $\alpha$-$MoO_3$ nanosheet. b) The channel current ($I_D$) dependence of the gate voltage under vacuum condition (<$10^{-5}$ Torr). Inset: The schematic illustration of the device structure and measurement setup. c–e) Schematic of the transistor structure corresponding to the gate voltage application. (c) Under the positive gate voltage, Li ions are accumulated at the channel surface building a concentration gradient field $E_{int}$ and then injected into the channel, resulting in the channel conductance increase. (d) The accumulated Li ions are driven back to the electrolyte by the build-in field $E_{int}$ at $V_G = 0$. (e) Under negative gate voltage, Li ions are extracted from the $\alpha$-$MoO_3$ channel, resulting in the channel conductance decreasing back to the initial state.

increase in low frequency region (<10 kHz) might involve two types of processes generated at the electrolyte/$MoO_3$ interface, the formation of electric double layer (EDL) without interfacial electrochemistry (0.3–10 kHz) and with the interfacial electrochemical processes (0.1–0.3 kHz). The ideal EDL without interfacial electrochemistry achieves large capacitance through the ion migration and then accumulation at the interface. It is an electrostatic process and becomes constant with frequency declining to a certain value. In contrast to the ideal EDL capacitance, the EDL with interfacial electrochemical processes involves the ions injecting into the channel, that is, electrochemical doping, where Faradaic charges ($Q_F$) pass through the interfaces resulting in an additional pseudocapacitance. Since pseudocapacitance is a slower process, the effective capacitance value usually keeps increasing with decreasing the frequency, and can be described by a phenomenological relationship $C = (1/2)\sigma^{-1}f^{-1/2}$ ($\sigma$ is a parameter related with the Warburg impedance).[49] Therefore, the second growth of capacitance in lower frequency region (0.1–0.3 kHz), as shown in Figure 2a, is predominantly attributed to the EDL with electrochemical doping.

The electrochemical doping could also occur during the EDL formation (0.3–10 kHz) under the dc bias, because $Q_F$ transferred through EDL interfaces in a surface redox process are always a function of gate potential and the derivative, $dQ_F/dV$, then causes pseudocapacitance. To prove that, the dc voltage dependence of capacitance in the Au/electrolyte/$MoO_3$ structure was performed. Figure 2b shows the $V_G$ dependence of capacitance at several frequencies. At 10 and 100 kHz, the capacitance displayed weak $V_G$ dependence. The capacitance at 2 kHz, however, increased significantly with increasing $V_G$, indicating the appearance of the pseudocapacitance. The total amount of accumulated charges $Q_T$ can be evaluated by the integration of the $C$–$V_G$ curves, that is, $Q_T = \int C\,dV_G = Q_M + Q_F$, where $Q_M$ is the mobile charge. As shown in Figure 2c, the total charges from $C$–$V_G$ integration at 10 and 100 kHz are almost same, indicating electrostatic nature of the interface charging, where $Q_F$ can be neglected at these frequencies and the total charges is equal to the mobile charges. When the frequency decreased to 2 kHz, the total charge becomes larger. There are two sources for the charge increase. One is the interfacial EDL formation and the other is the Faraday charge-transfer processes (i.e., electrochemical doping). Assuming that the Faraday charge transfer can be ignored at $V_G = 0$ V, the density of the $Q_F$ can be estimated from the difference between the integration

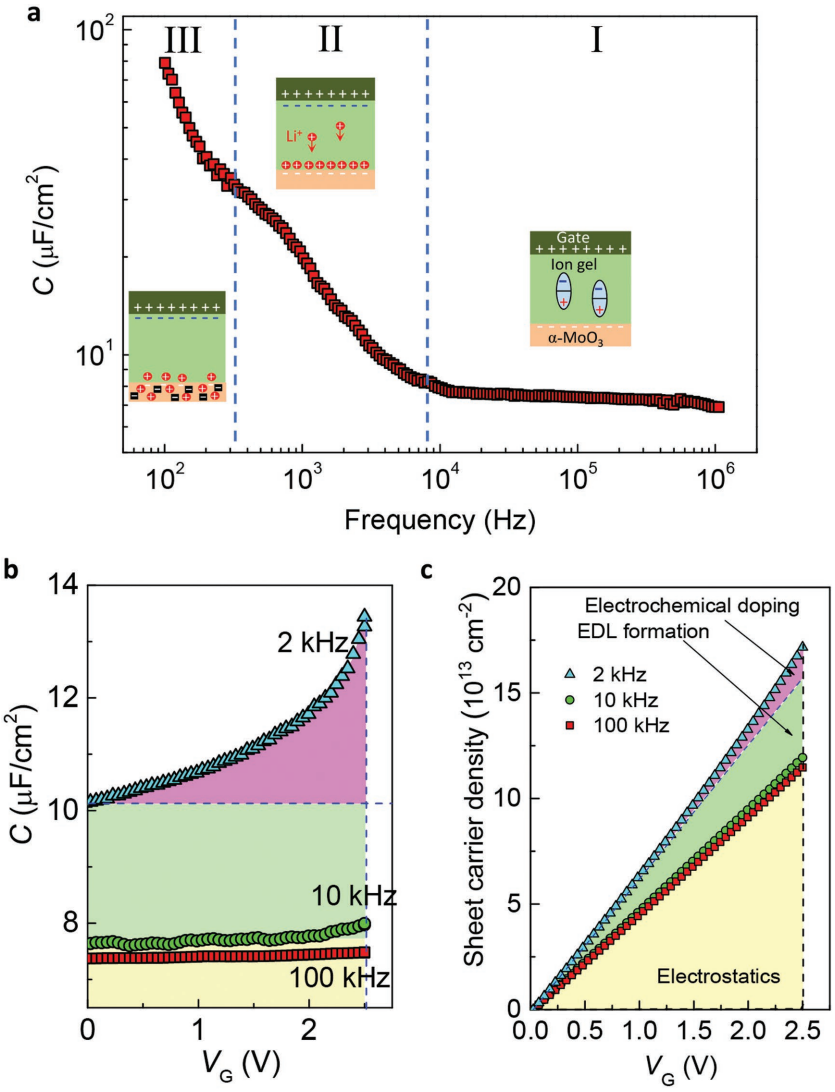


**Figure 2.** a) Specific capacitance as a function of applied frequencies. Region I: bulk electrolyte charging. Region II: EDL charging. Region III: pseudocapacitance charging. b) Specific capacitance as a function of applied bias. c) Comparison of interface charge density estimated from the $C$–$V_G$ integration.

of $C$–$V_G$ curve ($17.2 \times 10^{13}$ cm$^{-2}$ at 2.5 V) and the integration of constant $C$ when $V_G = 0$ V ($15.7 \times 10^{13}$ cm$^{-2}$ at 2.5 V), namely $1.5 \times 10^{13}$ cm$^{-2}$ at 2.5 V or 0.02 electrons per $\alpha$-$MoO_3$ unit cell.

### 2.2. Emulation of Synaptic Plasticity

The analogy between a biological chemical synapse and the $\alpha$-$MoO_3$-based ECT is depicted in **Figure 3**a. Biological chemical synapses can be classified by the type of cellular structures serving as the pre- and postsynaptic components.[50] These include but not limited to axodendritic synapse (axon terminal ends on a dendrite spine), axoaxonic synapse (axon terminal secretes into another axon), axosomatic synapse (axon terminal ends on soma), and axosynaptic synapse (axon terminal ends on another axon terminal). Structurally, the three-terminal $\alpha$-$MoO_3$-based ECT is analog to the axodendritic synapse. The gate mimics an axon that delivers spikes from a preneuron to the presynaptic membrane and the $\alpha$-$MoO_3$ channel combined with a drain electrode mimics a biological dendrite. The mobile $Li^+$ in the ion gel moves in the electric field analogous to the neuron transmitters in the synaptic cleft that induces an excitatory postsynaptic current (EPSC) in the dendrite through the contact of postsynaptic membrane. The connection strength between the axon and dendrite, that is, synaptic weight, is reflected by the EPSC intensity.

As shown in Figure 3b, a series of voltage pulses with the same duration time (10 ms) and different amplitudes (1.0, 1.5, 2.0, and 2.5 V) were applied on the gate electrode as external action potential, and the corresponding EPSC is measured using a fixed source–drain voltage (50 mV). The EPSC attained a peak value, which increased with increasing amplitudes of voltage pulses, at the end of the pulse and then decayed back. This behavior is similar to that observed in biological excitatory synapses.[51] With increasing the pulse amplitude to 2.0 and 2.5 V, the EPSC does not decay back to the resting current value (≈2.9 nA), indicating nonvolatility (see Figure 3d). The channel current read at 100 s after the gate voltage pulse stimulation was defined as the final value ($I$) and the nonvolatile portion can be calculated by $((I - I_0)/I_0) \times 100\%$, where $I_0$ is the initial channel current value. Moreover, the EPSC is also influenced by the duration time of the voltage pulses. As shown in Figure 3c,e, the nonvolatile portion increases (decreases) with increasing (decreasing) the pulse duration time. The volatile and nonvolatile behaviors of the channel conductance can be understood based on the capacitive nature and electrochemical doping of Li ions in the transistor, respectively. Under the voltage pulses with low amplitudes or short duration times, the Li ions in the electrolyte are just accumulated at the channel surface, playing the role of EDL to induce charge carriers in the channel. When removing the gate voltage, the accumulated Li ions diffuse back to the electrolyte due to the ion concentration gradient potential, resulting in the decay of the channel conductance to the resting value. Voltage pulses with higher amplitudes or long duration times induce electrochemical doping (Equation (1)), forming molybdenum bronze and leading to a nonvolatile change of the channel conductance.

It is crucial for neuromorphic computing that the transistors operate with a competitive energy efficiency. Because the "write" operation is decoupled from the "read" process and the "write" current (i.e., gate current) is lower than the "read" one, the energy efficiency of the $\alpha$-$MoO_3$-base synaptic transistor is "read" limited with a value comparable to "read" energies of

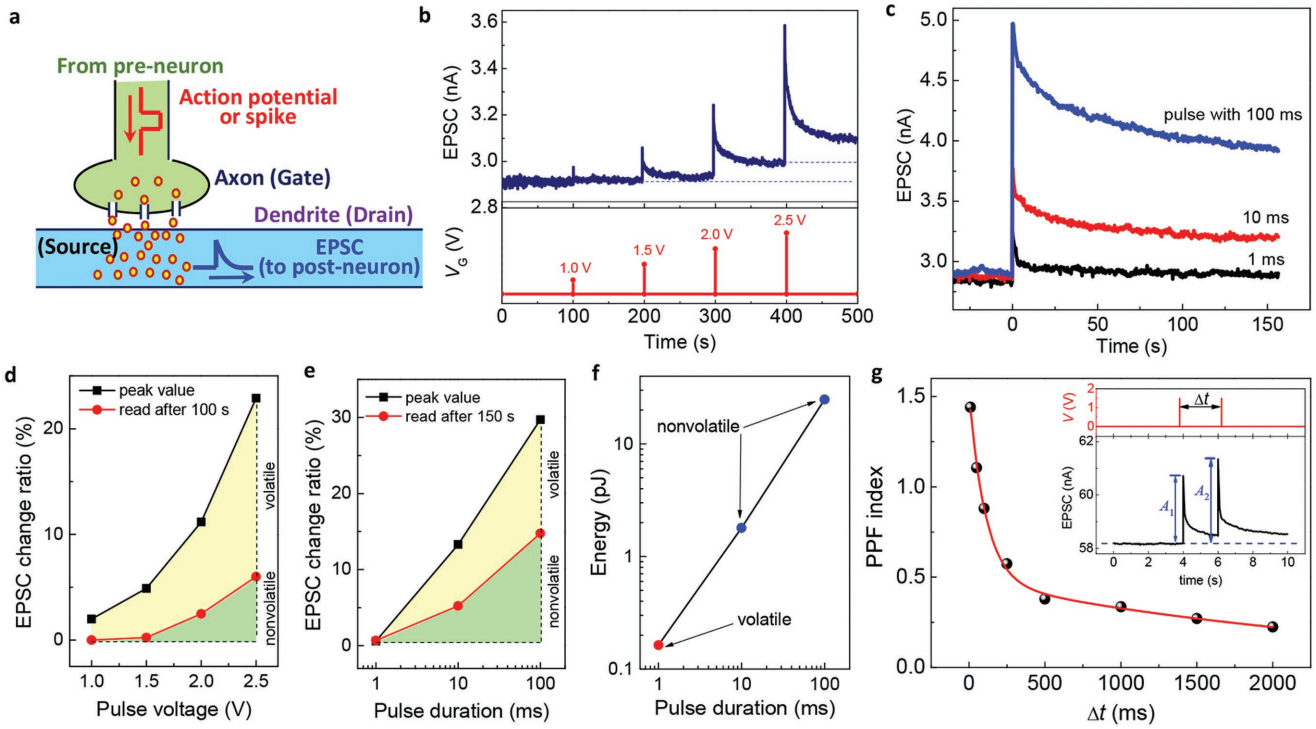


**Figure 3.** a) Schematic illustration of a biological axodentritic synapse. The plasticity between a pair of pre- and postneurons is modulated by the action potential or spikes from preneuron, inducing EPSC in postneuron for signal transmission and storage. The gate, source–drain, and channel conductance of the $\alpha$-$MoO_3$-based ECT act as the axon of the preneuron, the dendrite of the postneuron, and synaptic weight, respectively. b) EPSC stimulated by a series of gate voltage pulses with the same duration time (10 ms) and different amplitudes (1.0, 1.5, 2.0, and 2.5 V). c) EPSC stimulated by gate voltages with the same amplitude (2.5 V) and different duration times (1, 10, 100 ms). d) Pulse amplitude dependence of the EPSC change ratio, $((I - I_0)/I_0) \times 100\%$, where $I_0$ and $I$ are the channel current before and after the gate voltage pulse stimulation, respectively. e) Pulse duration dependence of the EPSC change ratio. f) Pulse duration dependence of the energy consumption for a single pulse (2.5 V) event. g) PPF index, defined as $(A_2 - A_1)/A_1$, where $A_1$ and $A_2$ are the amplitudes of the first and second EPSCs, plotted as a function of pulse interval ($\Delta t$). Inset: the EPSC stimulated by a pair of gate voltage pulses with $\Delta t = 2$ s.

the devices. Therefore, the energy consumption for a single pulse event can be evaluated by $I_p \times V_D \times t$, where $I_D$, $V_D$, and $t$ are the peak value of the EPSC, the drain voltage, and the pulse duration, respectively. The minimum value for the volatile and nonvolatile conductance change are 0.16 and 1.8 pJ for a single pulse (2.5 V) event (see Figure 3f), respectively, which are orders of magnitude lower than those of conventional CMOS circuit (several hundreds of picojoules per spike),[6] however comparable to (or higher partially than) that of reported three-terminal artificial synaptic devices (see **Table 1**). Note that the present channel area of our synaptic transistors is large (≈10 μm). Scaling down the devices to sub-micrometer scale could further reduce the energy consumption to several tens of femtojoules per spike, which is comparable to the biological synapse in the brain (≈10 fJ per spike).[7]

The volatile and nonvolatile change of the channel conductance in the $\alpha$-$MoO_3$-based ECT can be used to emulate the short- and long-term synaptic plasticity characteristics, respectively, which are separated by the retention times of the synaptic weight.[52] Paired-pulse facilitation (PPF) is a form of short-term plasticity and was reported to be important for decoding temporal information in the biological system.[53] It depicts a phenomenon in which conductance stimulated by the second spike is increased when the second spike closely follows the first one. Figure 3g shows the channel conductance change stimulated by a pair of voltage pulses (1.5 V, 10 ms) with a pulse interval ($\Delta t$) of 2 s. The peak value of the channel conductance stimulated by the second pulse is larger than that by the first one. The PPF index, defined as the ratio of the amplitude changes between the first EPSC value (*A*1) and the second EPSC value (*A*2), is plotted as a function of $\Delta t$ in the inset of Figure 3g. The PPF index decreases gradually with increasing $\Delta t$. This behavior was fitted by a double-exponential function with two characteristic timescales, $\tau_1 = 110$ ms and $\tau_2 = 2624$ ms, which are comparable to those measured in biological synapses.[54]

Long-term synaptic plasticity characteristics, such as the long-term potentiation (LTP) and long-term depression (LTD) of synaptic weight, are essential to implement neuromorphic computational functions in low energy operation. As shown in **Figure 4**a, by alternatively applying 50 identical pulses (+/−2.5 V, 10 ms) with 10 s space, bidirectional analog switching was obtained, where the channel conductance was set to numerous states between 42 and 75 nS in both the conductance rising and falling processes. The obtained channel conductance shows nonvolatile behavior, where each channel conductance decays to a stable value different from the previous one (see Figure 4b). Thus, the channel conductance increase and decrease can be regarded as the synaptic LTP and LTD, respectively. Symmetric

**Table 1.** Materials and switching properties in electrochemical transistors. MEH-PPV, poly[2-methoxy-5-(20-ethylhexyloxy)-*p*-phenylene vinylene]; PEDOT:PSS, poly(3,4-ethylenedioxythiophene):polystyrene sulfonate; KCl, potassium chloride; PEG, polyethylene glycol; LiPON, lithium phosphorous oxynitride; $LiClO_4$, lithium perchlorate; PEO, polyethylene oxide; P3HT, poly(3-hexylthiophene-2,5-diyl); Ion gel, poly(styrene-*block*-methyl methacrylate-*block*-styrene) triblock copolymer and 1-ethyl-3-methylimidazolium bis(trifluoromethyl sulfonyl) imide in ethyl acetate; Ionic liquid, 1-ethyl-3-methylimidazolium bis-(trifluoromethanesulfonyl)-imide; PEI, poly(ethylenimine).

| Channel material | Electrolyte | Active ions | Linearity of weight update | Conductance[a)] | Operation energy[b)] | Ref. |
|---|---|---|---|---|---|---|
| p-Si | $RbAg_4I_5$/MEH-PPV | $Ag^+$ | – | ≈130 nS | ≈10 pJ | [34] |
| Indium zinc oxide | $SiO_2$ | $H^+$ | – | ≈26 nS | ≈45 pJ | [32] |
| PEDOT:PSS | KCl | $H^+$ | – | ≈750 µS | – | [36] |
| Carbon nanotube | PEG | $H^+$ | – | ≈45 nS | ≈7.5 pJ | [33] |
| $ZnO_x$ | $Ta_2O_5$ | $O2^-$ | ≈0.7 | ≈35 nS | ≈35 pJ | [35] |
| $WSe_2$ | $LiClO_4$/PEO | $Li^+$ | ≈0.15 | ≈570 pS | 30 fJ | [41] |
| PEO/P3HT | Ion gel | – | ≈0.25 | ≈0.28 nS | ≈1.23 fJ | [40] |
| $\alpha$-$MoO_3$ | Ionic liquid | $H^+$ | ≈0.2 | ≈95 nS | ≈0.2 pJ | [37] |
| PEDOT:PSS/PEI | KCl | $H^+$ | ≈0.1 | ≈850 µS | ≈10 pJ | [39] |
| $Li_{1-x}CoO_2$ | LiPON | $Li^+$ | ≈0.1 | ≈250 µS | – | [38] |
| $\alpha$-$MoO_3$ | $LiClO_4$/PEO | $Li^+$ | ≈0.31 | ≈75 nS | ≈0.16 pJ | This work |

[a)]The devices display both a low and a high conductance state, where the high conductance state is selected; [b)]The energy will scale with channel area.

synaptic weight update behavior between the LTP and LTD is an important factor for designing synaptic devices which directly affects learning accuracy of neuromorphic computing systems.[20–25] A desired performance for synaptic devices is the linear conductance change between the LTP and LTD processes. To illustrate this performance of the $\alpha$-$MoO_3$-based ECT,

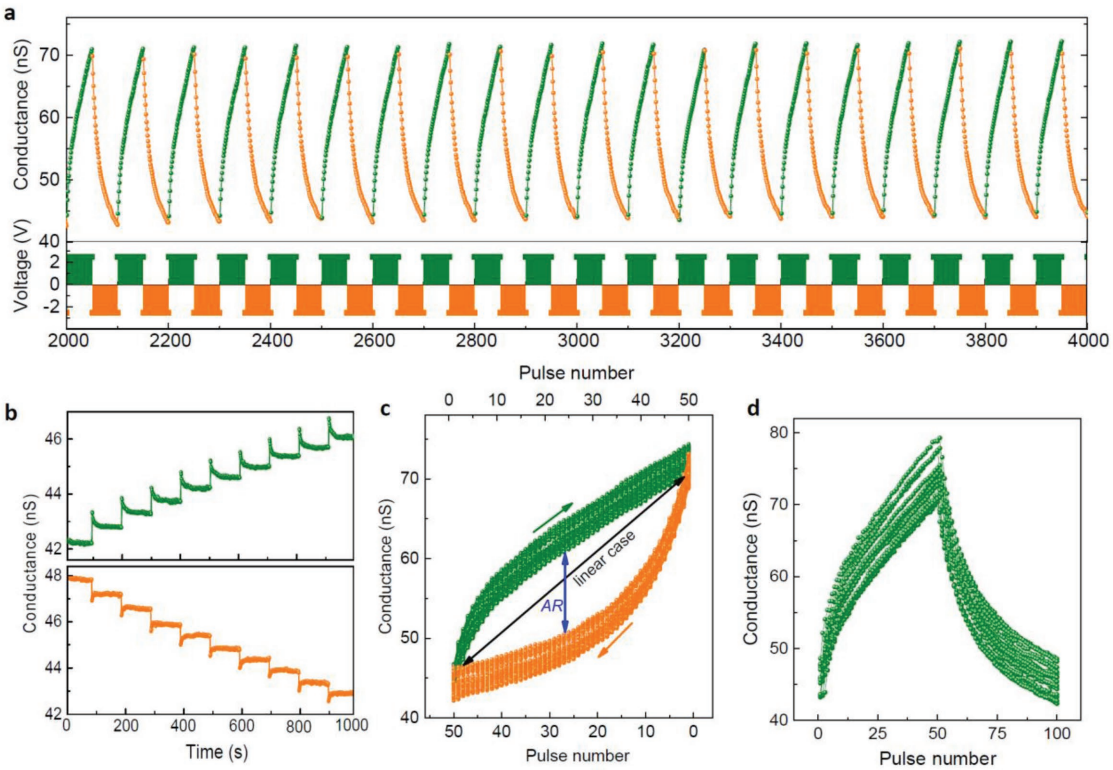


**Figure 4.** a) Analog channel conductance modulation under 50 repeated positive (2.5 V for 10 ms spaced 10 s apart) and negative (–2.5 V for 10 ms spaced 10 s apart) gate voltage pulses. The channel conductance values were read out 10 s after the pulse application. The channel conductance increase and decrease emulate the LTP and LTD of biological synapse, respectively. b) Retention of the derived channel conductance states for LTP (top panel) and LTD (bottom panel). The conductance is measured for 100 s after a gate voltage pulse (±2.5 V for 10 ms). c) The condensed plot of the LTP and LTD processed over 50 cycles, by which the asymmetric ratio (AR) between the LTP and LTD and temporal variation are calculated. d) The condensed plot of the LTP and LTD of 15 $\alpha$-$MoO_3$-based ECT, by which the device-to-device variation is calculated.

the 50 cycling LTP and LTD results are condensed together and replotted in Figure 4c. The asymmetric ratio (AR) can be defined as

$$\mathrm{AR} = \frac{\max\left|G_{\mathrm{P}}(n) - G_{\mathrm{D}}(n)\right|}{G_{\mathrm{P}}(50) - G_{\mathrm{D}}(50)} \quad \text{for } n = 1 \text{ to } 50 \tag{2}$$

where $G_P$(n) and $G_D$(n) are the channel conductance values after the $n$th potentiation pulse and $n$th depression pulse, respectively. AR should be zero for an ideal symmetric case. The calculated AR value of the synaptic transistor is 0.31 ± 0.12, which is well below that of two-terminal memristive devices triggered by identical pulses (0.55–0.88).[20–25] Note that an almost-linear weight update (AR ≈ 1) was obtained in a Ag/SiGe/Si two-terminal memristive device recently by confining the conductive filament in engineered, 1D dislocations.[55] Compared with the reported synaptic transistors, the AR value is still higher (see Table 1). To further improve the linearity of the synaptic transistors, one promising way is to improve the ion capacity of the channel materials as well as channel conductance sensitivity to doping to further enhance the channel conductance change ratio. By intentionally moderating the injection of ions, the conductance saturation could be suppressed at the expense of the conductance change ratio and then the linearity could be improved.

The cycle-to-cycle variation, i.e., write noise, was characterized by measuring the change of the channel conductance derived by applying the same gate voltage over 50 switching cycles. The maximum variations are as low as 6.5% and 9.3% for LTP and LTD, respectively. 15 synaptic transistors were prepared by using $\alpha$-$MoO_3$ nanosheets with the thickness of 16.8–28.0 nm, corresponding to 12–20 layers. The LTP and LTD measurements show that the device-to-device variations is <12% (see Figure 4d), indicating good device-to-device uniformity of our devices. It should be point out that the main limitation of mechanical exfoliation technique is that it cannot be implemented on a large scale, for example, for larger array devices. In view of the proposed operation mechanism of the synaptic transistors, however, it is possible to realize similar functionality by using polycrystalline thin film of $\alpha$-$MoO_3$ which can be prepared largely by other thin film deposition techniques such as magnetic sputtering.

### 2.3. Neuromorphic Computing Simulation

An artificial neural network has been simulated using the experimentally measured long-term plasticity characteristics to perform supervised learning with back-propagation of two different data sets: a small image version (8 × 8 pixels) of handwritten digits from the "Optical Recognition of Handwritten Digits" dataset and Modified National Institute of Standards and Technology (MNIST) dataset, a large image version (28 × 28 pixels) of handwritten digits.[56,57] Backpropagation is a widely used method for benchmarking synaptic array architectures with the data sets.[22] In the simulation, CrossSim, a three-layer network (one hidden layer) is used for backpropagation, as shown in **Figure 5**a. Figure 5b shows schematically a crossbar array of a synaptic weight layer. The $\alpha$-$MoO_3$-based synaptic transistors act as a memory element in a crossbar array and their channel conductance change was used as the weight update for executing the backpropagation algorithm. Here, the crossbar is considered as part of a "neural core" that executes vector-matrix multiplication (inference) and outer-product updates (learning) operations as described previously.[38,39,58] In order to properly simulate the device nonideality, the probability distribution of the change in channel conductance ($\Delta G$) induced by a potentiation or depression pulse was recorded (Figure 5c,d). By sampling from the probability distribution during weight updates to the crossbar, the device noise, nonlinearity, and asymmetry were accounted for. The recognition accuracies of the simulated networks after each training epoch are plotted in Figure 5e,f. The results of the training are compared to an identical network with ideal floating-point numeric precision which represents the neuromorphic algorithm limit and provides an important benchmark. For recognizing small, handwritten digits, the recognition accuracy approaches 90% within the second training epoch and approaches 94.1% (96.7% as a maximum of ideal numeric training) after 40 training epochs. The performance is within 3% of ideal accuracy. For recognizing large, handwritten digits, the recognition accuracy approaches 87.3% and the performance deviated by as much as 10% of the ideal accuracy. Although the recognition accuracy is lower than that of other two-terminal memristors and three-terminal synaptic devices (>95%),[38,39,55] the simulation proves that the neural network formed with $\alpha$-$MoO_3$-based synaptic transistor has better performance than what is typically found in two-terminal resistive switching memories (20–70%) and the phase change memory devices (82.2%).[20–23,58] Note that a phase change memory–based artificial neural network has reached the accuracy of 98% recently by combining long-term storage in phase change memory playing the long-term synapses' role and near-linear updates of volatile transistors and capacitors playing the short-term synapses' role.[59] The nonlinearity and asymmetry of the conductance update in programming will ultimately degrade network accuracy. To achieve higher network accuracy, further improvements to the $\alpha$-$MoO_3$-based synaptic transistor are still required.

Although the recognition accuracy of the simulated neural network and linear conductance tuning behavior are not particularly improved, a clear improvement of the $\alpha$-$MoO_3$-based synaptic transistor for neuromorphic computing is the ultralow conductance (<75 nS) compared with that of the reported two-terminal memristive devices[11–25,58] and part of synaptic transistors (see Table 1). The low device conductance is highly required for use in crossbar arrays. For example, in order to support a 1000 × 1000 crossbar with a fully parallel write/read operation, each synaptic device can load no more than a maximum current of 10 nA (corresponding to 200 nS at 50 mV) because the scaled wires at 10 nm half pitch can only handle 10 μA before electromigration becomes an issue.[60] Moreover, higher operating current also causes the unacceptable parasitic voltage drops and excessive energy dissipation on wires. Therefore, given the low operating currents required, the $\alpha$-$MoO_3$-base synaptic transistors with the ultralow conductance are promising for future application of neuromorphic networks composed of large-scale device arrays.

In addition to the low conductance, it is essential for synaptic transistors to operate with a competitive speed during

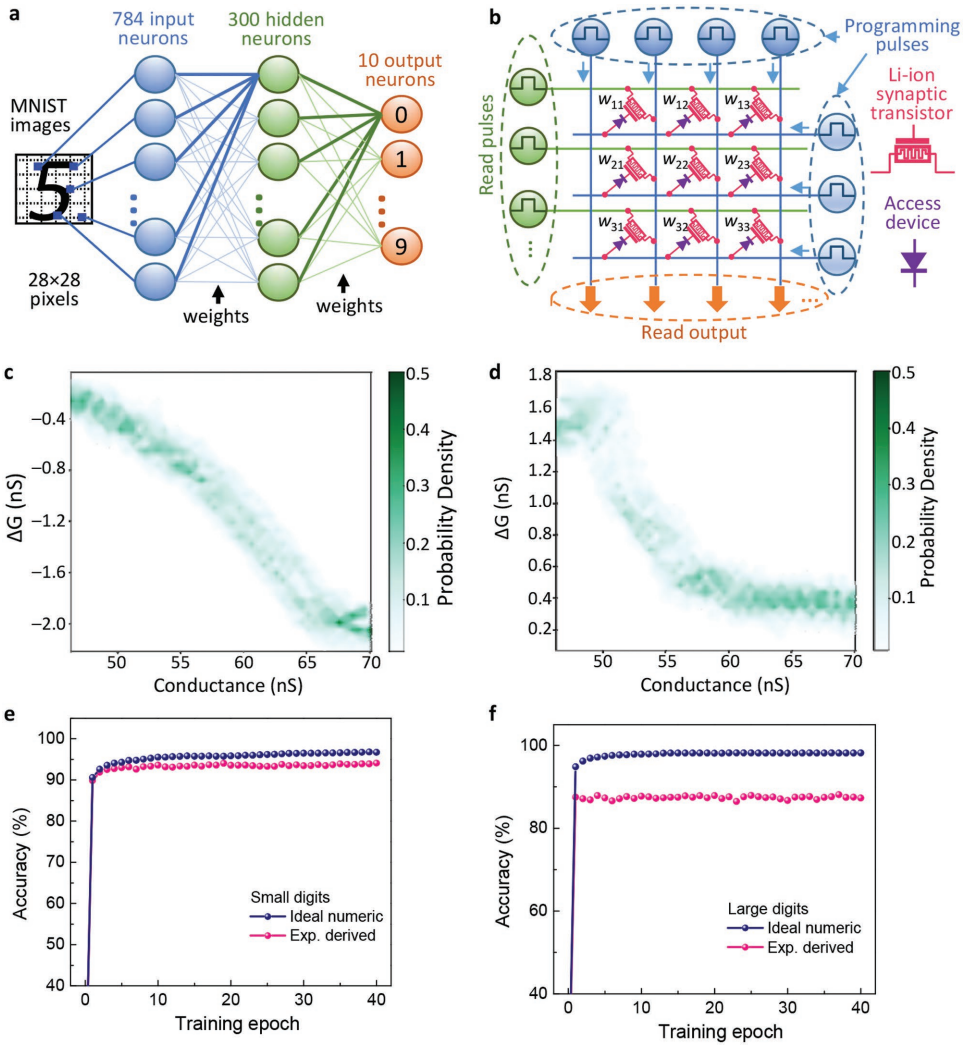


**Figure 5.** a) Schematics of a three layer (one hidden layer) neural network. b) Schematics of a synaptic weight layer composed of voltage programmed Li-ion synaptic transistor crossbar array and access devices. c,d) The probability distribution of channel conductance change ($\Delta G$) induced by one gate voltage pulse versus the initial conductance during potentiation (c) and depression (d). The statistics were collected from 5000 switching events. The CrossSim uses them to model both the write noise and write nonlinearity for training simulation. e,f) The recognition accuracy evolution with training epochs for $8 \times 8$ pixel handwritten digit image (e) and $28 \times 28$ pixel handwritten digit image (f).

neuromorphic computing. The operation speed of our synaptic transistors is slower than that of two-terminal memristive devices (<100 ns). Figure 2a reveals that the cutoff frequency for the occurrence of electric double layer is ≈10 kHz, meaning that the pulse duration for the electric double layer formation with Li-ion intercalation process can be as short as 0.1 ms under appropriate gate voltage. This speed may not be a problem for off-line training process, but may have an adverse impact on online training. Improving operation speed is still a challenge for electrochemical transistors because it is related to ion drift and diffusion in gate electrolyte. Since charge-transfer process is usually fast enough, the speed of electrochemical doping is mainly limited by the ion diffusion in the channel. To improve the operation speed, it we suggest to select gate electrolytes and channel materials with high ion mobility to shorten the duration time for ion migration. Furthermore, the switching speed could also be increased through further scaling down the device dimensions, especially reducing the channel and electrolyte thickness to shorten the ion diffusion distance. Compared with the planar configuration of the transistor, vertical configuration might be more convenient for meeting these requirements.

## 3. Conclusion

In summary, we have described an ECT that emulates an artificial synapse based on reversible Li-ion intercalation into layered 2D $\alpha$-$MoO_3$ nanosheets. The short- and long-term plasticity, bidirectional analog, and near-symmetric weight update between LTP and LTD have been achieved with ultralow channel conductance values (<75 nS) essential for high energy efficiency. Neural network simulations demonstrate that crossbar arrays based on these synaptic transistor arrays will

achieve 94.1% recognition accuracy of handwritten digit data sets. The successful implementation of synaptic functionalities lies in the filament-free switching mechanism where Li ions are reversibly intercalated into the $\alpha$-$MoO_3$ lattice through electrochemical doping processes. Similar ionic processes can be implemented in other layered 2D oxides that exhibit redox-related conductivity. These results provide an attractive approach to utilize 2D oxide-based ECT devices for large-scale, energy-efficient neuromorphic computational networks.

## 4. Experimental Section

*Synthesis of $\alpha$-$MoO_3$ Single Crystal*: $\alpha$-$MoO_3$ single crystals were prepared on a glass substrate by the vapor phase transport method. A ceramic boat with $MoO_3$ power (99.9% Alfa Aesar) and the glass substrate was placed in two temperature zones of a horizontal tube furnace, respectively. Then, the $MoO_3$ zone was heated to 720 °C at a rate of 5 °C $min^{-1}$ and maintained for 3 h in argon gas with a flow rate of 100 sccm $s^{-1}$, and the substrate zone was held at 150 °C. The $\alpha$-$MoO_3$ single crystals with dimensions up to a few millimeters in length and width, and 0.5 mm in thickness were collected for the mechanical exfoliation. 15 $\alpha$-$MoO_3$ nanosheets with the thickness of 16.8–28.0 nm, corresponding to 12–20 layers were obtained and were used to prepare synaptic transistors. The X-ray diffraction ((XRD) pattern and high resolution transmission electron microscopy (HRTEM) image show that it had good orthorhombic single crystal structure.[37]

*Mechanical Exfoliation of $\alpha$-$MoO_3$ Nanoflakes*: Scotch tape was attached to the as-prepared $\alpha$-$MoO_3$ single crystal. By repeated peeling it off, the $\alpha$-$MoO_3$ single crystal was cleaved into various sheets with few layers. The tape was attached to the $SiO_2$ (300 nm)/Si substrate, which had been treated by plasma beforehand to increase the adhesion of the $\alpha$-$MoO_3$ nanosheets. Then, the tape was peeled off swiftly, and a large number of $\alpha$-$MoO_3$ nanosheets with thicknesses less than 20 nm were obtained on the $SiO_2$/Si substrate.

*Fabrication of the Synaptic Transistor Device*: Electron-beam lithography was used to pattern the contacts of the $\alpha$-$MoO_3$ nanosheets onto the $SiO_2$/Si substrate to form lateral three-terminal devices. Cr/Au (5/60 nm) contact electrodes were deposited via thermal evaporation. The devices were annealed in vacuum ($10^{-5}$ Torr) at 200 °C for 1 h in order to remove resist residues and enhance the metallic contacts. $LiClO_4$ (Sigma-Aldrich) dissolved in PEO ($M_w$ = 100 000, Sigma-Aldrich) matrix was used as the gate solid dielectric. $LiClO_4$ and PEO powders (0.3 and 1 g, respectively) were mixed with 15–30 mL anhydrous methanol. The mixture was stirred for 24 h at 50 °C and then dip-coated on the device surface.

*Electrical Measurement*: The gate voltage application and drain current monitor were achieved by a measurement system including two Keithley 2611 Source Meters. The scan speed of gate voltage was 25 mV $s^{-1}$. The capacitance measurement was performed by an LCR meter (Agilent 4980A) with an applied ac voltage of 0.5 V and frequency range from 100 Hz to 2 MHz. All the electrical measurements were carried out on a homemade sample stage in an enclosed chamber, which was pumped below $10^{-5}$ Torr in the overall measurement. Additionally, the devices were annealed in the vacuum chamber at 110 °C for 2 h to eliminate residual methanol and moisture.

*Array Simulation*: The simulation was conducted on the basis of the platform CrossSim.[38,39,58] It provides a clean python application programming interface (API) so that different algorithms can be built upon resistive memory crossbars while modeling realistic device properties and variability. A three-layer (one hidden layer) neural network was used to execute supervised learning over the training examples after which the network accuracy was compared against the test examples in a single training epoch. The simulations took into account the device nonidealities as well as analog to digital (A/D) and digital to analog (D/A) conversion by "external electronics" that interfaced with the crossbar by sending voltages and summing currents along the rows and columns. The network simulations were carried out on two data sets: a small image version (8 × 8 pixels) of handwritten digits from the "Optical Recognition of Handwritten Digits" dataset and MNIST dataset, a large image version (28 × 28 pixels) of handwritten digits. For small digit images, the network size was 64 × 36 × 10. After training with 3823 images, a separate 1797-image testing set was used for recognition. For MNIST images, the network size was 784 × 300 × 10. After training with 60 000-image training set, a separate 10 000-image testing set was used for recognition.

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## Conflict of Interest

The authors declare no conflict of interest.

## Keywords

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