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Electric gating of the multichannel conduction in $LaAlO_3/SrTiO_3$ superlattices*

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Electric gating of the multichannel conduction in $LaAlO_3/SrTiO_3$ superlattices*

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The electric gating on the transport properties of two-dimensional electron gas (2DEG) at the interface of $LaAlO_3/SrTiO_3$ (LAO/STO) heterostructure has attracted great research interest due to its potential application in field-effect devices. Most of previous works of gate effect were focused on the LAO/STO heterostructure containing only one conductive interface. Here, we systematically investigated the gate effect on high-quality LAO/STO superlattices (SLs) fabricated on the TiO_2-terminated (001) STO substrates. In addition to the good metallicity of all SLs, we found that there are two types of charge carriers, the majority carriers and the minority carriers, coexisting in the SLs. The sheet resistance of the SLs with a fixed thickness of the LAO layer increases monotonically as the thickness of the STO layer increases. This is derived from the dependence of the minority carrier density on the thickness of STO. Unlike the LAO/STO heterostructure in which minority and majority carriers are simultaneously modulated by the gate effect, the minority carriers in the SLs can be tuned more significantly by the electric gating while the density of majority carriers is almost invariable. Thus, we consider that the minority carriers may mainly exist in the first interface near the STO substrate that is more sensitive to the back-gate voltage, and the majority carriers exist in the post-deposited STO layers. The SL structure provides the space separation for the multichannel conduction in the 2DEG, which opens an avenue for the design of field-effect devices based on LAO/STO heterostructure.

Keywords: superlattices, gate effect, minority carriers, majority carriers

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1. Introduction

Since the high mobility two-dimensional electron gas (2DEG) at oxide interfaces between $LaAlO_3$ (LAO) and $SrTiO_3$ (STO) was discovered first by Hwang *et al.*,[1,2] the LAO/STO heterostructure has been a focus of intensive studies in recent years due to its exotic properties, including coexisting 2D superconductivity[3] and 2D magnetism,[4–6] strong gate effect,[7] and Rashba spin–orbit coupling effect.[8,9] It is intensively involved in the researches on spintronics, such as spin current generation, spin to charge conversion, and spin transport.[10,11] Among those novel physical properties, the gate effect is of special interest due to its analogous structure to the field-effect devices, which is the footing stone of semiconductor industry. The switching from low-resistance to high-resistance has been achieved in LAO/STO heterostructure by applying a gate voltage.[7] Caviglia *et al.*[8] also discovered that the magnitude of Rashba spin–orbit interaction existing in LAO/STO heterostructure can be modulated by an external electric field, derived from the change of the carrier density.

However, these works mainly focused on the simple LAO/STO heterostructure with only one conductive interface. In recent years, some attempts have been devoted to the fabrication of the heterostuctures containing multiple conductive interfaces. Lee *et al.*[12] prepared a STO/LAO/STO(001) multilayer film, in which a p-type interface formed of 2D hole gas is achieved besides the n-type interface. In addition, Kim *et al.*[13] reported the nonlinear Hall effect and multichannel conduction generated by the electronic reconstruction in the δ-doped $LaTiO_3/SrTiO_3$ superlattices (SLs).

Despite above progresses, the works to study this system including multiple conductive heterointerface are still scarce, especially the gate effect in LAO/STO SLs. Herein we report on the fabrication of high-quality LAO/STO SLs with different thickness of LAO and STO in each stacking periodicity on the TiO_2-terminated STO(001) substrate. The electric properties, such as the dependence of the sheet resistance (R_s) on temperature (T) (R–T curves) and Hall resistance (R_{xy}), were measured. The coexistence of two types of carriers (minority carriers and majority carriers) was confirmed in the SL samples. In addition, the gate effect of these SLs was systemati-

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cally investigated. The minority carriers show significant gate tunability by the backgate voltage, while the majority carrier density is nearly unchanged. We find that most of the minority carriers reside at the first interface in the STO substrate and most of the majority carriers exist in the post-deposited STO layers. This space separation between the majority carriers and minority carriers in the SL structure provides an avenue for the design of field-effect devices based on LAO/STO heterostructure.

2. Experimental details

The [STO(m)/LAO(n)] superlattice samples were epitaxially grown on TiO_2-terminated (001) $SrTiO_3$ substrate ($5\times5\times0.5$ mm^3) by pulsed laser deposition (PLD). Here, m or n denotes the thickness of each STO or LAO layer in unit cells (u.c.), respectively. The stacking periodicity of all the SLs is 8. Four different superlattices ([STO(5)/LAO(5)], [STO(4)/LAO(5)], [STO(3)/LAO(5)], and [STO(5)/LAO(3)]) were prepared for investigation. To get atomically flat TiO_2-terminated layer, the STO substrate was chemically etched by a $HCl-HNO_3$ acidic solution and then annealed at 1000 °C for 1 h in 1 bar oxygen atmosphere. Then, the SLs were prepared by PLD, monitored by the reflected high-energy electron diffraction (RHEED) *in situ*. The substrate temperature is 750 °C and the deposition oxygen pressure of the chamber is 10^{-5} mbar. The energy of pulse fluence (KrF excimer laser, 248 nm) is 1.5 J/cm^2 and the repetition rate is 1 Hz. After the deposition, the sample was cooled to room temperature at a rate of 10 °C/min with the constant oxygen pressure of 10^{-5} mbar. For comparison, the LAO single film with a thickness of 5 u.c. was also deposited on TiO_2-terminated (001) $SrTiO_3$ substrate ($5\times5\times0.5$ mm^3) under the same condition, i.e., LAO/STO heterostructure.

The surface morphology of the SLs was measured by the atomic force microscope (AFM, SPI 3800N, Seiko). The crystal structure of the films was determined by the Bruker diffractometer (D8 Discover, Cu K_α radiation). Resistive measurements were conducted in the Quantum Design physical property measurement system (PPMS). The van der Pauw geometry was adopted for the measurement and ultrasonic aluminum (Al) wire bonding was used for electric contact. The measurement current is 10 μA. To tune the carrier density of the samples, a gate bias was applied at the backside of STO through a copper electrode, and the upper LAO/STO SLs were grounded by the ultrasonic Al wire.

3. Results and discussion

The RHEED patterns before and after the growth of the SLs are given in Figs. 1(a) and 1(b). The sharp RHEED peaks can be clearly seen, indicating the high crystal quality of the substrate and LAO/STO SLs. Figures 1(c) and 1(d) show the oscillation of the RHEED intensity during the deposition of the SLs which clearly reveals the layer-by-layer epitaxial growth of LAO and STO films. Figure 1(e) shows the typical morphology of the [STO(5)/LAO(5)] sample. The image size is 5×5 μm^2. The regular steps with the height difference of 1 u.c. prove the atomically-flat surface of the as-prepared sample. The x-ray diffraction (XRD) patterns of four SL samples are shown in Fig. 1(f). Besides the main reflection peak at $\sim47.2°$, satellite peaks corresponding to the superlattices structure (marked by above numbers) are clearly demonstrated. With increased thickness of the SLs in one stacking periodicity, the distance between the main peak and satellite peaks decreases. Moreover, the finite-size oscillations due to the finite layer thickness (the peaks marked by triangles between the main diffraction peak and satellite peaks) are also observed. All these features indicate the high quality of the as-prepared SLs.

Figure 2 compares the electric transport properties of all SLs and the LAO/STO heterostructure prepared under the same condition. Figure 2(a) is the temperature (T) dependence of the sheet resistance. All samples show the metallic characteristic with a weak upturn at low temperature, which is usually attributed to the Kondo effect. The resistance of the SLs is lower than that of the LAO/STO heterostructure including only one conductive interface. For the SL samples with a fixed thickness of 5 u.c. for the LAO layer, the sheet resistance decreases with the thickness of STO from 5 u.c. to 3 u.c. at low temperature. To get the information of carrier density and mobility, the Hall resistance of all samples was also measured at different temperatures. The R_{xy}–H curves of [STO(5)/LAO(5)], [STO(4)/LAO(5)], and [STO(3)/LAO(5)] show nonlinear dependence on the magnetic field in the low temperature region (<100 K). Figure 2(b) shows the Hall resistance of [STO(5)/LAO(5)] from 2 K to 300 K. We attribute the nonlinear dependence to the multiple carrier conduction, which usually derives from the complex band structure of STO constituting light and heavy mass bands crossing the Fermi level.[14,15] It is usually described as the two-band model,[16–18] in which the Hall resistance can be given by

$$R_{xy}=\frac{\sigma_1^2R_1+\sigma_2^2R_2+\sigma_1^2R_1\sigma_2^2R_2(R_1+R_2)B^2}{(\sigma_1+\sigma_2)^2+\sigma_1^2\sigma_2^2(R_1+R_2)B^2}B,$$

where R_i and σ_i are the Hall coefficient and conductivity of the i-th type of carrier, respectively. The magnetic field (B) from -7 T to 7 T is perpendicular to the surface of the SLs during the measurement of the Hall resistance. This equation is constrained by the longitudinal conductance at zero magnetic field expressed as

$$\sigma_{xx}(B=0)=\sigma_1+\sigma_2.$$

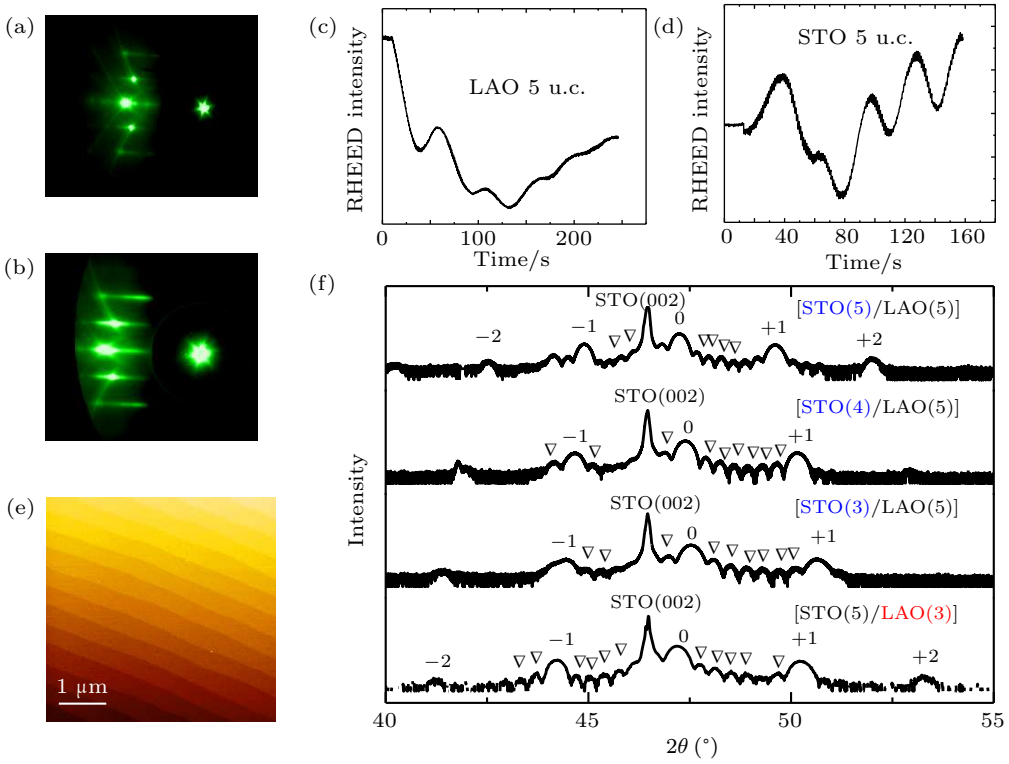

Fig. 1. (a), (b) The RHEED patterns before and after the deposition of the SLs, respectively. (c), (d) Typical RHEED spectra showing an intensity oscillation corresponding to the LAO growth and STO growth of the SLs ([STO(5)/LAO(5)]) in one period, respectively. (e) Morphology of [STO(5)/LAO(5)] measured by the atomic force microscope. (f) XRD patterns of all SLs in our experiment.

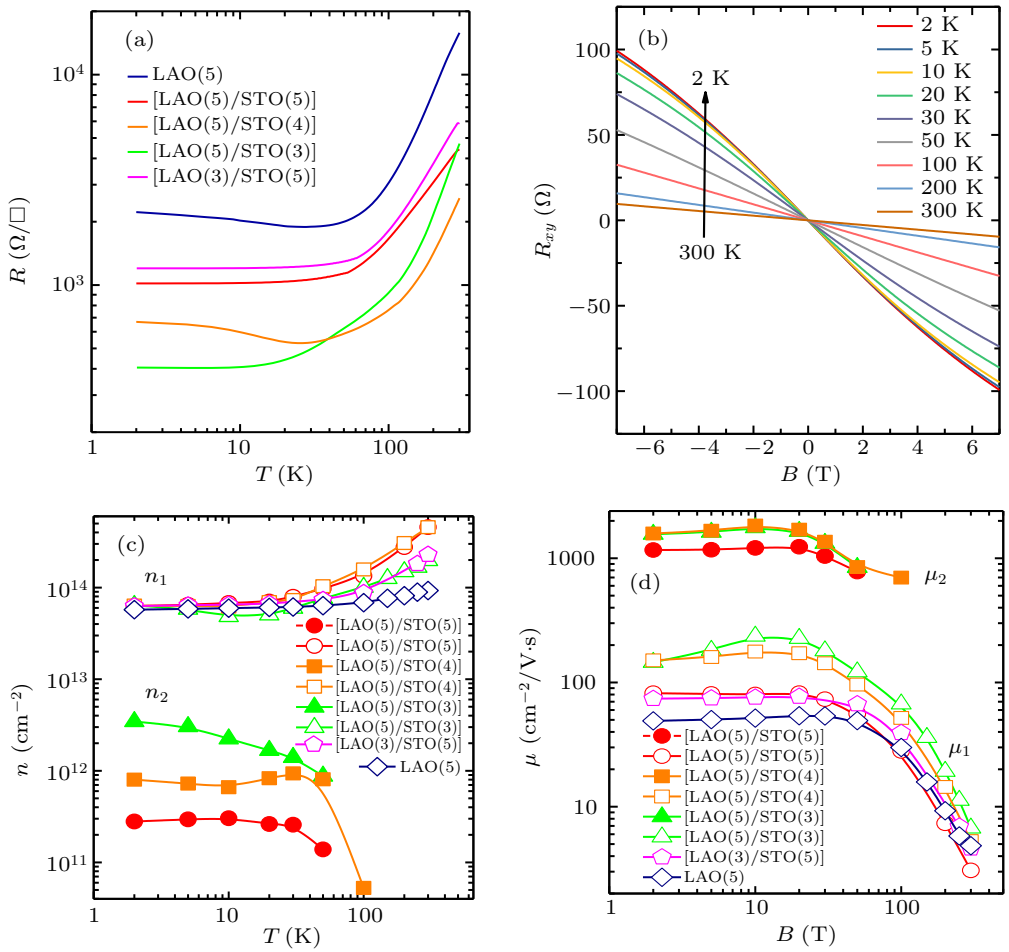

Fig. 2. (a) Temperature dependence of the sheet resistance for the SLs of different thickness and LAO/STO heterostructure. (b) Magnetic field dependence of the non-linear Hall resistance (R_{xy}) for [STO(5)/LAO(5)] measured at the temperature from 2 K to 300 K. (c), (d) Carrier density and mobility as a function of temperature determined by the Hall resistance, respectively.

Both of the carrier density (n_1) and mobility (μ_1) of majority carriers with high carrier density and the carrier density (n_2) and mobility (μ_2) of minority carriers with relatively low carrier density can be deduced by $\sigma_{1,2} = n_{1,2}e\mu_{1,2}$ and $R_{1,2} = -1/n_{1,2}e$. The carrier density and mobility of each sample at different temperature are acquired by fitting the Hall resistance in Figs. 2(c) and 2(d). At 300 K, the carrier density of SLs is greater than 5×10^{14} cm^{-2}, higher than $\sim 9\times10^{13}$ cm^{-2} of the LAO/STO heterostructure. As the temperature is reduced, the majority carriers of the SLs are frozen out, indicating the existence of the localized electrons. Especially, for the [STO(5)/LAO(5)] and [STO(4)/LAO(5)] SLs, the high density charge carriers decrease by approximately one order of magnitude from 300 K to 2 K, while the carrier density of LAO/STO is almost independent of the temperature. When the temperature is lower than 100 K, the minority charge carriers appear in the [STO(5)/LAO(5)], [STO(4)/LAO(5)], and [STO(3)/LAO(5)] samples. At 2 K, the density of minority carriers is 2.7×10^{11} cm^{-2}, 7.5×10^{11} cm^{-2}, and 3.4×10^{12} cm^{-2} for [STO(5)/LAO(5)], [STO(4)/LAO(5)], and [STO(3)/LAO(5)], respectively, and the majority carrier density is virtually identical to $\sim 6.3\times10^{13}$ cm^{-2}. Different from the independence of the majority carriers on the layer of STO in SLs, the density of minority carriers becomes higher as the thickness of the STO layer deceases from 5 u.c. to 3 u.c. This well explains the relation between the sheet resistance of SLs and the thickness of STO. As for the mobility of SLs, the mobility of the majority carriers grows rapidly with the decreasing temperature from 300 K to 2 K because of the reduced electron–phonon scattering and enhanced dielectric permittivity at low temperature. For the SLs, the mobility of majority carriers is about 100 cm^2/V·s, and the mobility of minority carriers is on the order of 10^3 cm^2/V·s.

To further identify the spatial distribution of the carrier in the SLs, a systematic investigation on the gating effect is desirable. Figure 3(a) is the experiment set-up for the electric gating measurement. The bottom electrode lies at the back side of the STO substrate, and the top electrode is located at the interface between the first LAO layer and the STO substrate. The carriers of the 2DEG can be tuned by electric gating through the capacity effect. The polarity of the bias voltage determines the different effect of electric gating. The positive gate voltage would increase the carrier density while the negative gate voltage depletes the carriers. In this case, the carrier density is extracted by integration over the gate voltage range

$$n_{\mathrm{s}}\left(V_{\mathrm{g}}\right) = n_{\mathrm{s}}\left(V_{\mathrm{g}} = V\right) + \frac{1}{eA}\int_{V}^{V_{\mathrm{g}}} C\,\mathrm{d}V,$$

where C is the capacity and A is the area of the capacitor. For our sample, the capacity C can be expressed as $C = \varepsilon_0\varepsilon_{\mathrm{r}}A/d$, where ε_0 and ε_{r} are the vacuum dielectric constant and the dielectric constant of the dielectric material, respectively. So the change of carrier density just depends on the variation of the gate voltage, which can be deduced as $\Delta n_{\mathrm{s}} = \varepsilon_0\varepsilon_{\mathrm{r}}\Delta V_{\mathrm{g}}/ed$ ($d = 0.5$ mm). As is well known, $SrTiO_3$ has a very higher dielectric constant of 20000 at low temperature.[19] When the change of gate voltage (ΔV_{g}) is ~ 100 V, the change of carrier density (Δn_{s}) is on the magnitude of $\sim 2\times10^{13}$ cm^{-2}. We performed a systematic investigation of the gating effect on the Hall resistance of [STO(5)/LAO(5)], [STO(4)/LAO(5)], and [STO(3)/LAO(5)] at 2 K. The carrier density as a function of the gate bias deduced from the R_{xy}–H curves is summarized in Fig. 3(b). The minority carriers show much stronger dependence on the gate voltage than the majority carriers. As the gate voltage is from maximum to minimum, the variation of the majority carrier density is less than 1×10^{13} cm^{-2}, which is much smaller than the theoretical value calculated above. However, the minority carriers with low density reduce more than one order of magnitude with the same change of gate voltage (ΔV_{g}). This experimental result is distinct from that of the LAO/STO heterostructure containing just one conductive interface,[20,21] but analogous to that of the δ-doped $LaTiO_3/SrTiO_3$ superlattices.[13] As shown in Fig. 3(a), the top electrode contacts deeply into the STO substrate, so the electric field applied through the back gate dominantly affects the first conductive interface near the substrate from the bottom. In the first conductive interface, the minority carriers are mostly affected by the gate electric field.[13]

To further confirm that, another SLs [STO(5)/LAO(3)] was fabricated under the same preparation condition. In general, when the thickness of LAO is 3 u.c., which is less than the threshold thickness (4 u.c.) of the conductive LAO/STO interface, the first interface is insulating. In other words, there are no sufficient charge carriers to support the conductivity at the first interface. Like other SLs in this experiment, the [STO(5)/LAO(3)] is also metallic from 300 K to 2 K presented in Fig. 2(a). The Hall resistance displays a well linear variation with the magnetic field, indicating that only one type of carriers (majority carriers) exist in the SLs. As shown in Fig. 2(c), the carrier density in [STO(5)/LAO(3)] is 6.3×10^{13} cm^{-2} at 2 K, which is comparable to that of [STO(5)/LAO(5)], [STO(4)/LAO(5)], and [STO(3)/LAO(5)]. For [STO(5)/LAO(3)], the total carrier density is independent of the gate biases, as shown in Fig. 3(b). This phenomenon validates that the charge carriers of [STO(5)/LAO(3)] only exist in the post-deposited STO layers originating from the oxygen vacancies instead of in the STO substrate, because in this experiment set-up for the gate effect measurement, the gate voltage only can tune the carriers existing in the STO substrate. More interestingly, for all SLs ([STO(5)/LAO(3)], [STO(5)/LAO(5)], [STO(4)/LAO(5)], and [STO(3)/LAO(5)]) in this experiment, the changing regularity and value of ma-

jority carriers resemble each other. Perhaps, compared with the single conductive interface system, the SLs with multiple conductive interfaces have different distribution of charge carriers. Most of minority carriers exist at the first interface from the bottom, and most of the majority carriers reside in the post-deposited STO film. In SLs, the majority carriers possibly separate from the minority carriers in space.

In addition, while the gate voltage cannot modulate the resistance of [STO(5)/LAO(3)], as presented in Fig. 3(c), the sheet resistance of [STO(5)/LAO(5)], [STO(4)/LAO(5)], and [STO(3)/LAO(5)] at low temperature exhibits strong gate tunability with the change of the gate voltage. Figure 3(d) shows the *R*–*T* curves under different gate voltages for [STO(5)/LAO(5)]. This phenomenon is consistent with the dependence of the carrier density in [STO(5)/LAO(3)], [STO(5)/LAO(5)], [STO(4)/LAO(5)], and [STO(3)/LAO(5)] on the gate bias. The minority carriers exist in [STO(5)/LAO(5)], [STO(4)/LAO(5)], and [STO(3)/LAO(5)]. However, [STO(5)/LAO(3)] has no minority carriers. So the existence of minority carriers in the SLs enhances the modulation of resistance with the change of gate voltage. The resistance upturn with saturation at ultra-low temperature is the typical feature of the Kondo effect. The positive back-gate voltage (200 V) causes a downward shift of the *R*–*T* curve, indicative of an improvement of the metallicity. The increased carrier density suppresses the Kondo scattering, thus restrains the resistance upturn. With the gate voltage changed to negative, the low temperature resistance becomes largely derived from the obvious reduction of the iterate carriers. We consider that the origin of the Kondo effect is the localized Ti magnetic moments which are locally screened by the anti-ferromagnetically coupled carriers.[4,22,23] As the carrier density becomes lower, the Kondo scattering is stronger, then the upturn of the resistance is more pronounced.

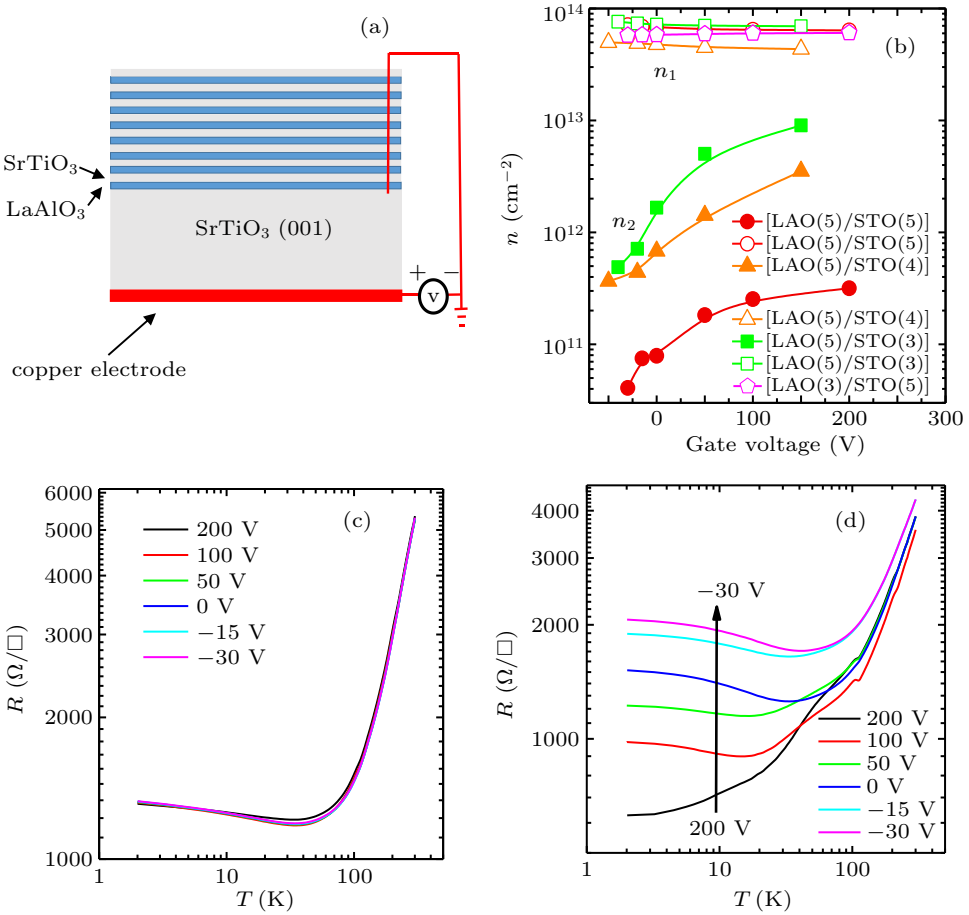

Fig. 3. (a) Experiment set-up for the gate-effect measurements of the superlattices. (b) The carrier density as a function of the gate voltage deduced from the Hall resistance. (c), (d) Gate effect on the *R*–*T* dependence of the samples [STO(5)/LAO(3)] and [STO(5)/LAO(5)], respectively.

4. Conclusion

In summary, high-quality 8-stacking-period LAO/STO SLs with different thickness of LAO and STO were fabricated. All SLs show satellite peaks corresponding to the SLs structure in the XRD patterns. The SLs show the better metallicity, compared to the LAO/STO including only one conductive interface. For the SLs with the thickness of LAO in one periodicity fixed at 5 u.c., in which the minority carriers and majority carriers coexist, their sheet resistance at 2 K decreases monotonically with the layers of STO reduced from 5 u.c. to 3 u.c., which is consistent with the dependence of the minor-

ity carrier density on the thickness of STO in each periodicity. By the gating effect measurement, we found that the appearance of minority carriers increases the variation of the resistance as a function of the gate bias. Unlike the LAO/STO heterostructure, the SL structure perhaps provides a different space separation for the multichannel conduction in the 2DEG. The minority carriers may mainly exist in the first interface near the STO substrate, and the majority carriers exist in the post-deposited STO layers. This work opens an avenue for the design of novel field-effect devices based on LAO/STO heterointerface.

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